EE 240 Circuits I

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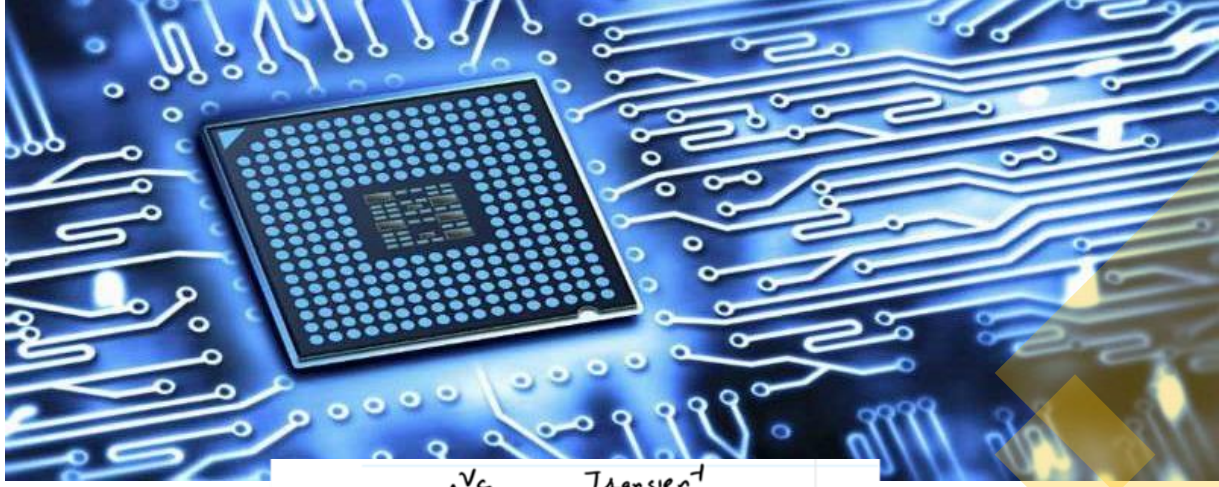
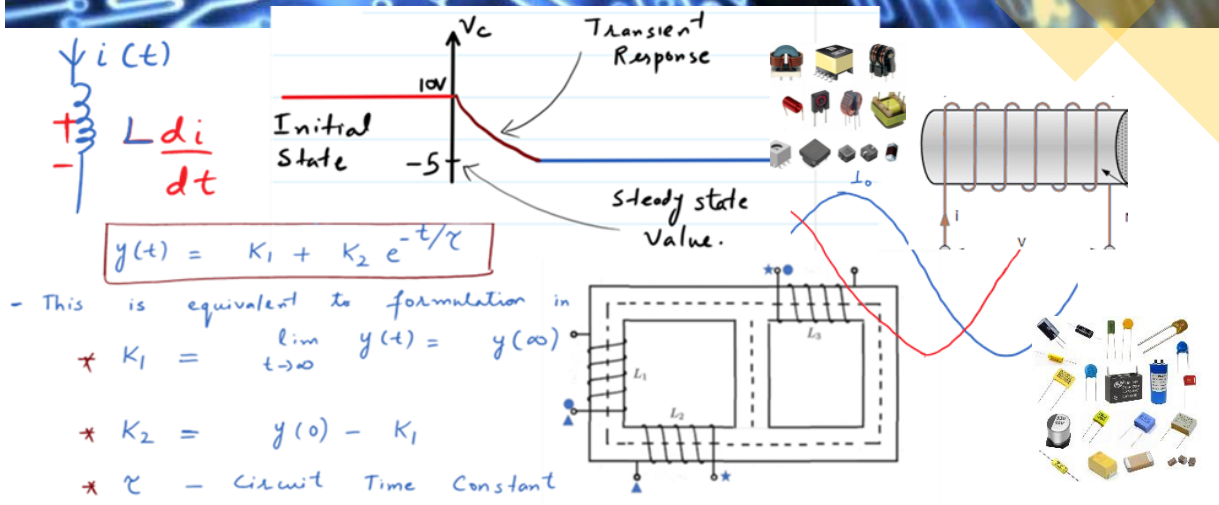
- Circuit Analysis
- Kirchhoff's Current Law (Nodal Analysis)
- Kirchhoff's Voltage Law (Loop Analysis)
- Examples





Circuit Analysis

Determine the current through or the voltage across every element in the circuit.

Big Picture: We will learn techniques to carry out circuit analysis in the following order.

Kirchhoff's Laws

- Formulation of equations for
  - Single node, single loop (R,L,C)
  - Multiple nodes or loops (R,L,C)
  - Coupled Circuits

- Nodal Analysis
  - Super Node
  - Resistive networks

- Loop Analysis
  - Super Loop
  - Resistive networks

- Matrix formulation of equations

- Equivalent Networks
  - Series parallel equivalent (already covered)
  - Source transformation

- Superposition Principle

- Concept of Duality

Circuit Analysis

Circuit:

Interconnection of circuit elements; passive elements and energy sources such that the energy flows between elements.

We analyse circuit by formulating network equations that is governed by Kirchhoff's Laws. These laws can be intelligently employed to formulate minimum number of independent equations. Before we formally define these laws, we quickly review the concepts node, loop, branch and ground node.

Node (Junction):

A point of connection of two or more circuit elements.

Loop:

Any closed path through the circuit in which no node is encountered more than once.

Branch:

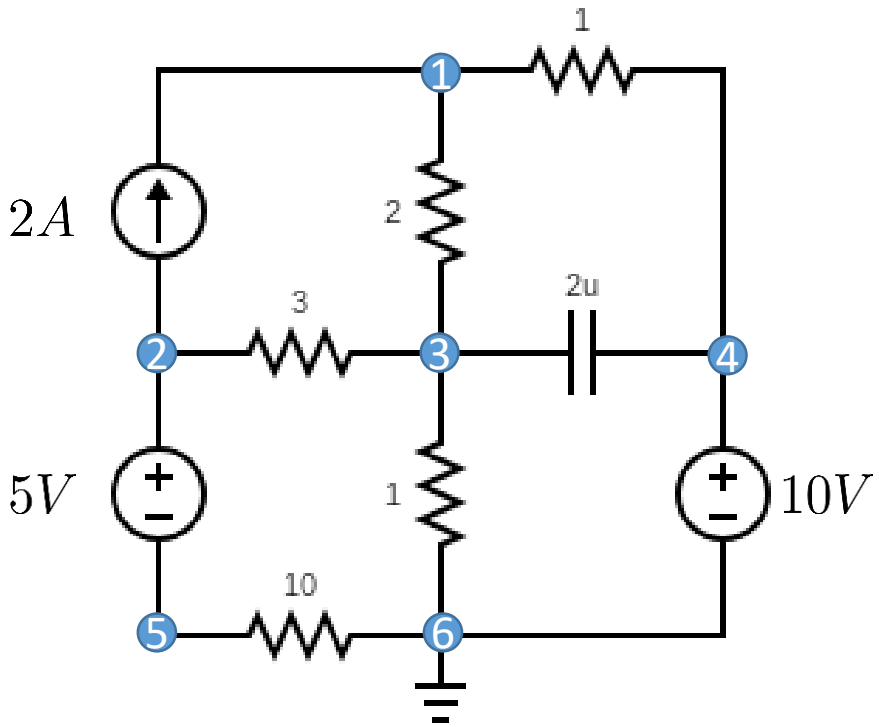
Part of circuit containing one element and nodes on both sides.

Ground, Zero potential node, Reference or Datum Node:

Since voltage in a circuit is a relative quantity, it is useful to have one reference node such that all the voltages are expressed with respect to the reference node.

Circuit Analysis

Example:



Interpretations:

- There are 6 nodes
- There are 9 branches
- We have considered node 6 as ground node
- Node 4 is at 10 V (with respect to ground node)
- 2A current is being drawn from node 2 and is being fed to node 1 through the branch connecting nodes 1 and 2.
- Node 2 is at 5V with respect to node 5

Kirchhoff's Current Law (KCL)

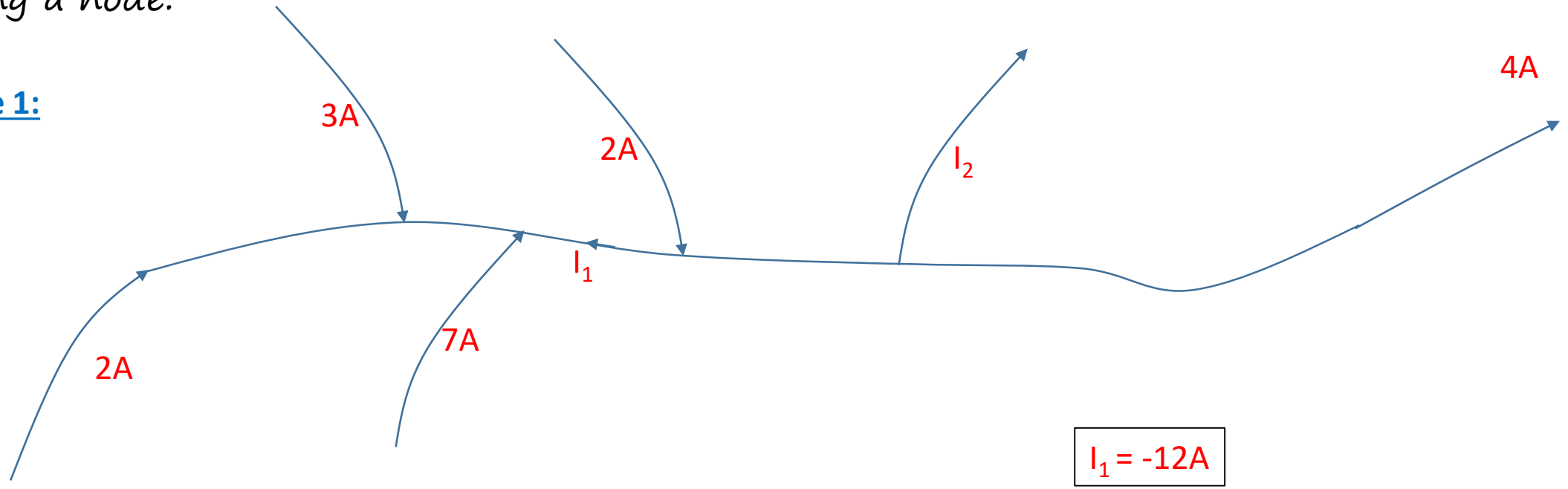
Statement:

Algebraic sum of all the currents entering (or leaving) a node is equal to zero.

OR

Algebraic sum of the currents leaving a node is equal the algebraic sum of the currents entering a node.

Example 1:



$I_1 = -12A$

$I_2 = 10A$

Nodal Analysis using Kirchhoff's Current Law

Steps:

- Define ground (reference) node
- Define the variables to indicate voltages at other nodes
- Apply KCL at each node to obtain equation associated with the node.
- Number of equations = number of nodes -1

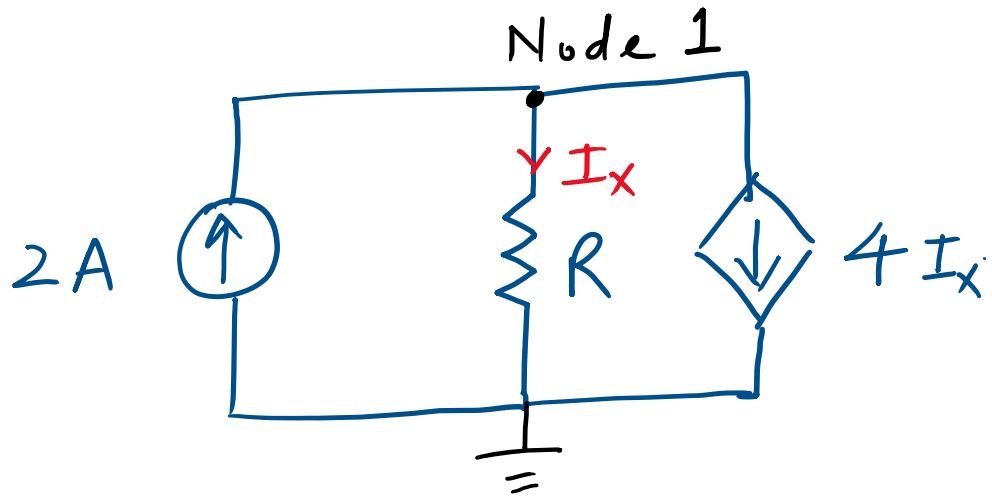
Example:
Single Node-Pair Circuit:

Determine I_x.

Applying KCL at node 1 yields

$$I_x + 4I_x - 2 = 0$$

$$I_x = \frac{2}{5} A$$



Nodal Analysis using Kirchhoff's Current Law

Example:

Single Node-Pair Circuit:

Determine I_1 and power absorbed by $6\,\Omega$ resistor.

Applying KCL at node 1 yields

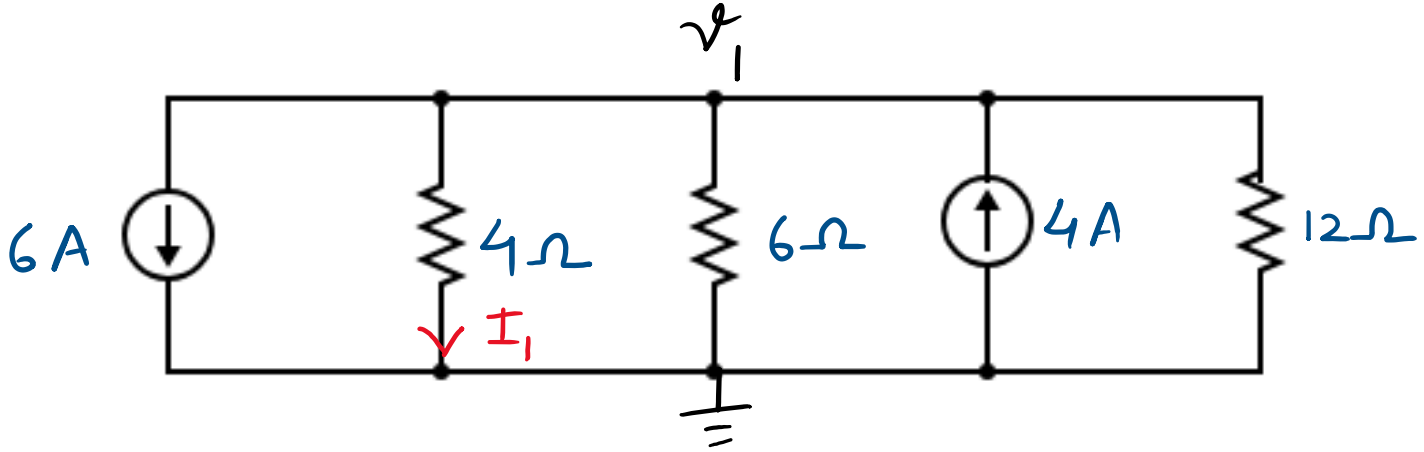
$$\frac{v_1}{4} + \frac{v_1}{6} + \frac{v_1}{12} + 6 - 4 = 0$$

$$v_1 = -4\,V$$

$$I_1 = \frac{v_1}{4} = -1\,A$$

Power absorbed by $6\,\Omega$ resistor

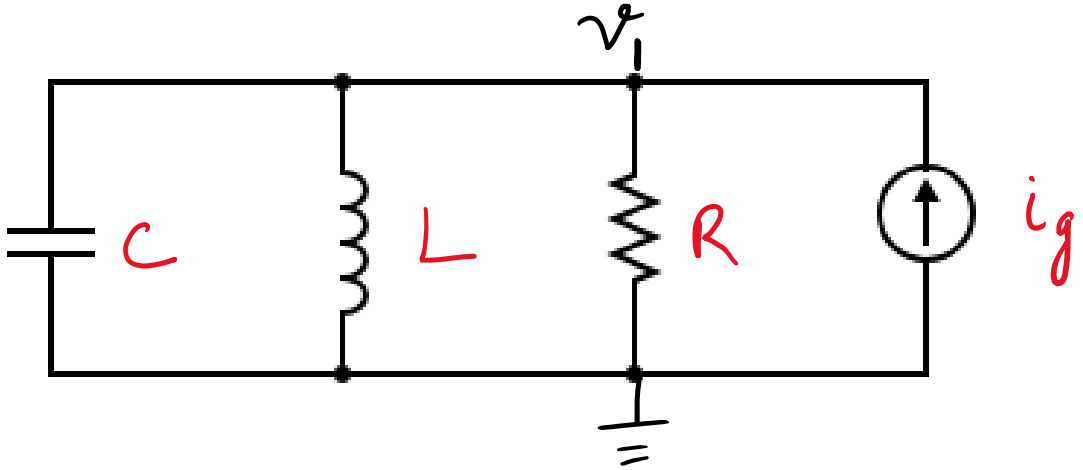
$$P_6 = \frac{v_1^2}{R} = \frac{16}{6}\,W$$



Nodal Analysis using Kirchhoff's Current Law

Example:

Single Node-Pair Circuit:

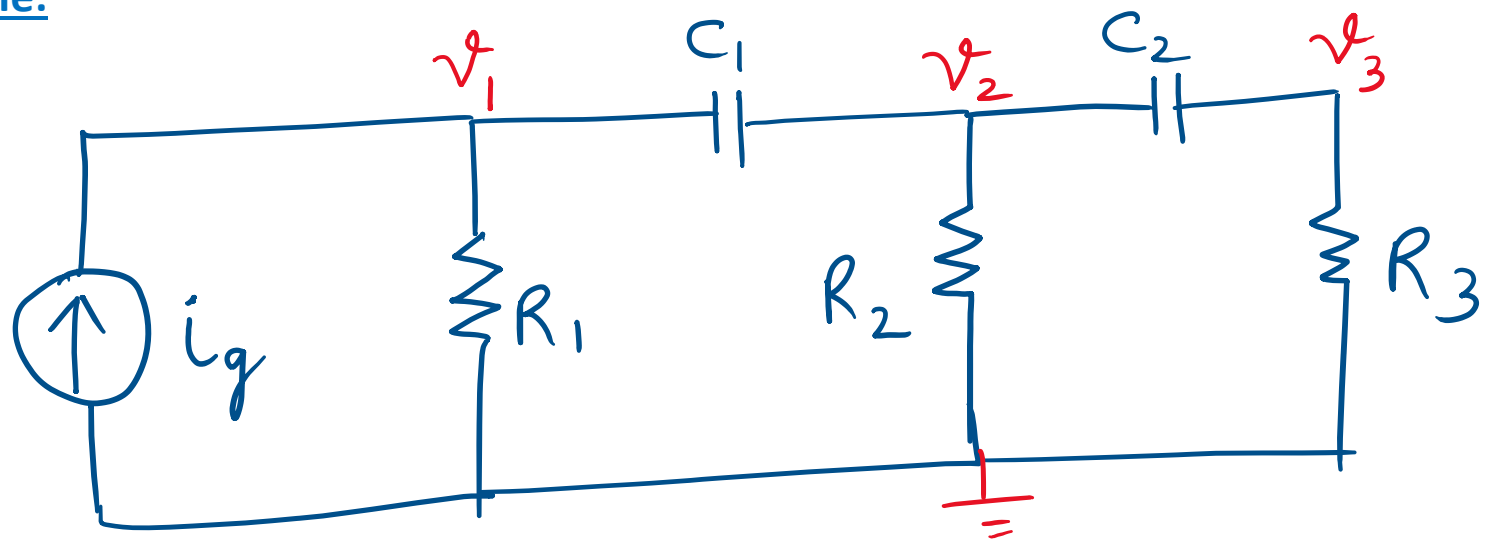


Parallel RLC Circuit

$$\frac{v_1}{R} + C\frac{d}{dt}v_1 + \frac{1}{L}\int v_1 dt - i_g = 0$$

Nodal Analysis using Kirchhoff's Current Law

Example:



Node 1: $\frac{v_1}{R_1} + C_1 \frac{d}{dt}(v_1 - v_2) - i_g = 0$

Node 2: $\frac{v_2}{R_2} + C_1 \frac{d}{dt}(v_2 - v_1) + C_2 \frac{d}{dt}(v_2 - v_3) = 0$

Node 3: $\frac{v_3}{R_3} + +C_2 \frac{d}{dt}(v_3 - v_2) = 0$

Kirchhoff's Voltage Law (KVL)

Statement:

Algebraic sum of all the drop (or gain) of voltages around any closed-path is equal to zero.

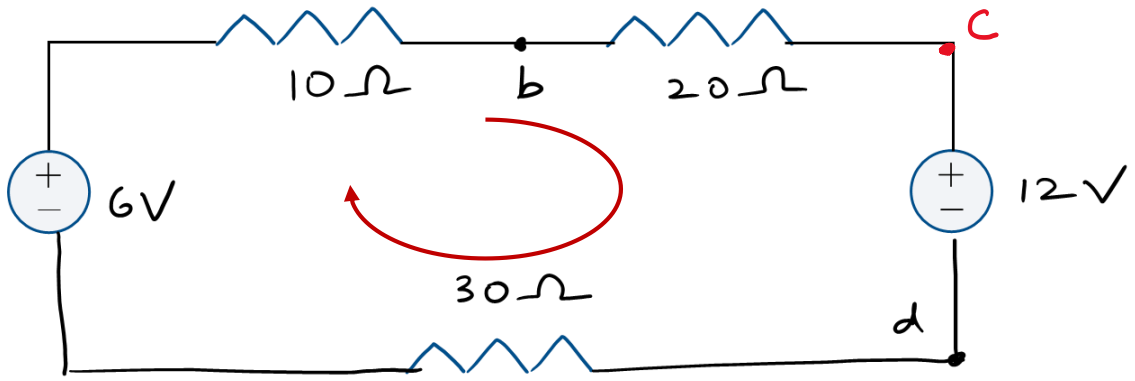
OR

Algebraic sum of the drop of voltages is equal the algebraic sum of the gain of voltages around a closed path.

Example:

Single Loop Circuit:

Determine V_{bd}.



$$10i + 20i + 12 + 30i - 6 = 0$$

$$\Rightarrow \quad i = \boxed{-0.1\,A}$$

$$v_{bd} = v_{bc} + v_{cd} = (20)(i) + 12 = \boxed{10V}$$

Loop Analysis using Kirchhoff's Current Law

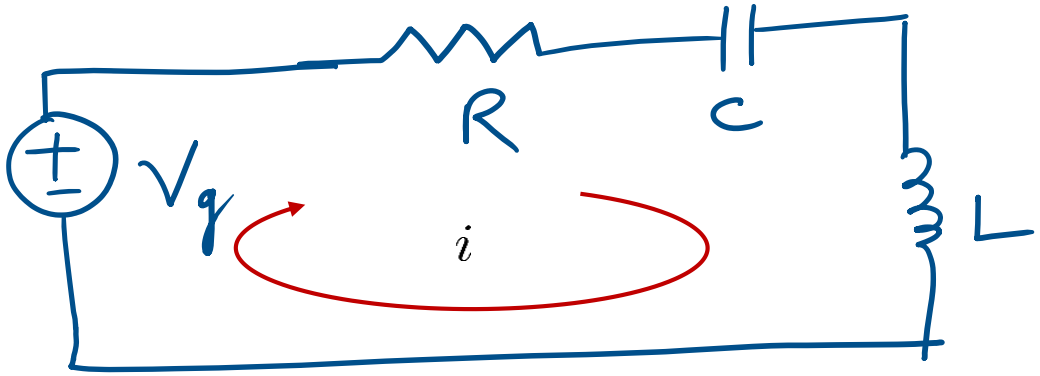
Steps:

- Define Loop (or mesh) currents (variable + direction)
- Apply KVL around each loop to obtain equation associated with the loop.
- Number of equations = number of nodes -1

Example:
Single Loop Circuit:

Formulate network equation.

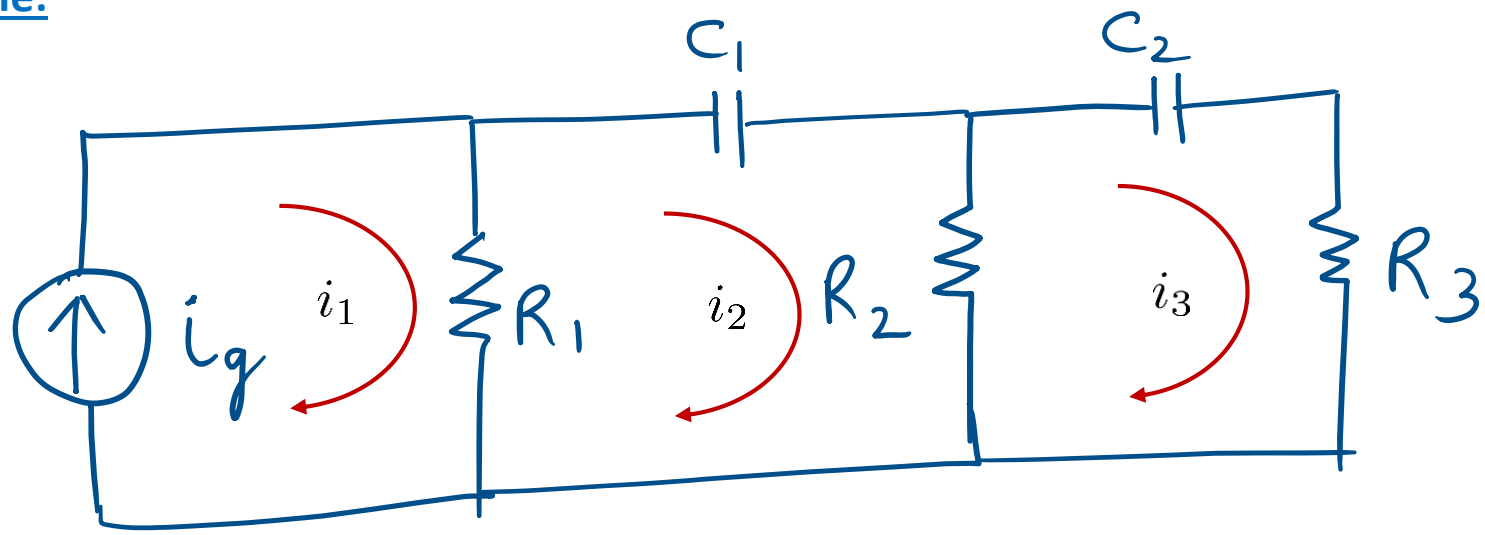
$$iR + L\frac{d}{dt}i + \frac{C}{L}\int idt - v_g = 0$$



Series RLC Circuit

Kirchhoff's Voltage Law

Example:



We have a current source in the loop 1 and therefore we know the loop current. We do not need to traverse the loop to write the equation.

Loop 1: $i_1 = i_g$

Loop 2: $$\frac{1}{C_1}\int i_2 dt + R_2(i_2 - i_3) + R_1(i_2 - i_1) = 0$$

Loop 3: $$\frac{1}{C_2}\int i_3 dt + R_3 i_3 + R_2(i_3 - i_2) = 0$$

Nodal Analysis

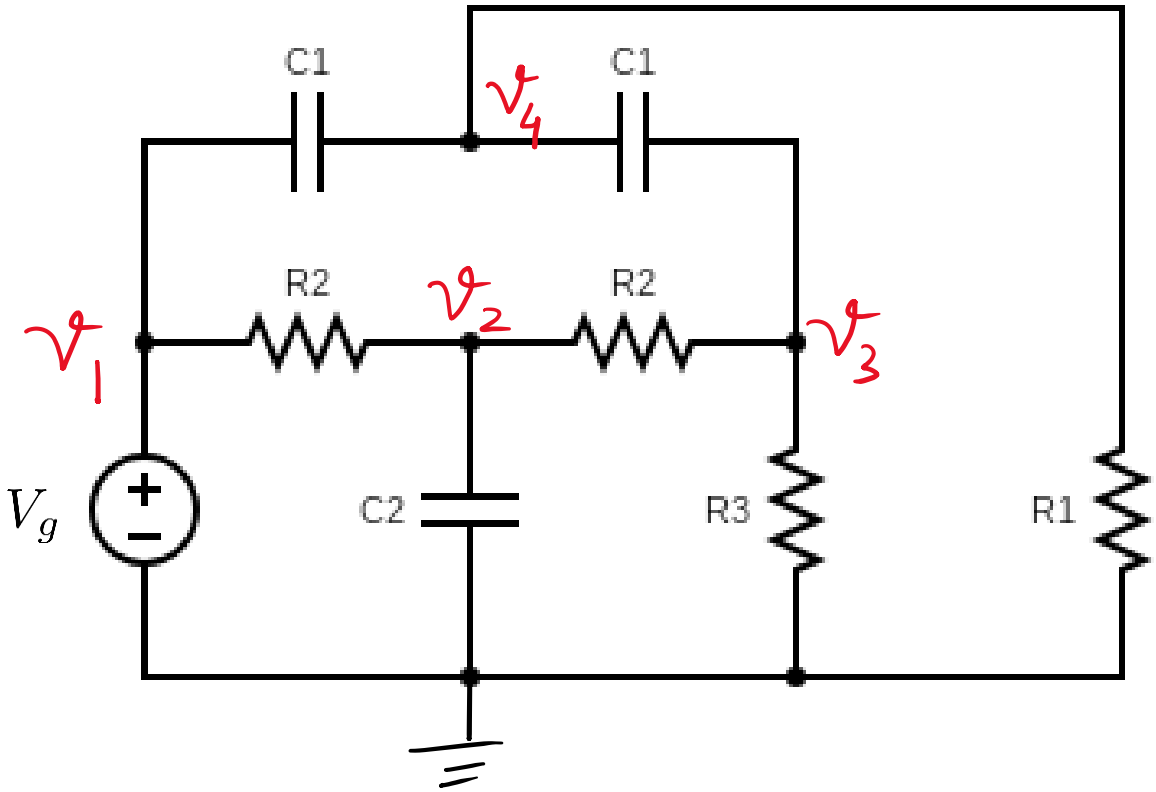
Reinforcement Example:

$$v_1 = V_g$$

$$\frac{v_2 - v_1}{R_2} + \frac{v_2 - v_3}{R_2} + C_2 \frac{d}{dt} v_2 = 0$$

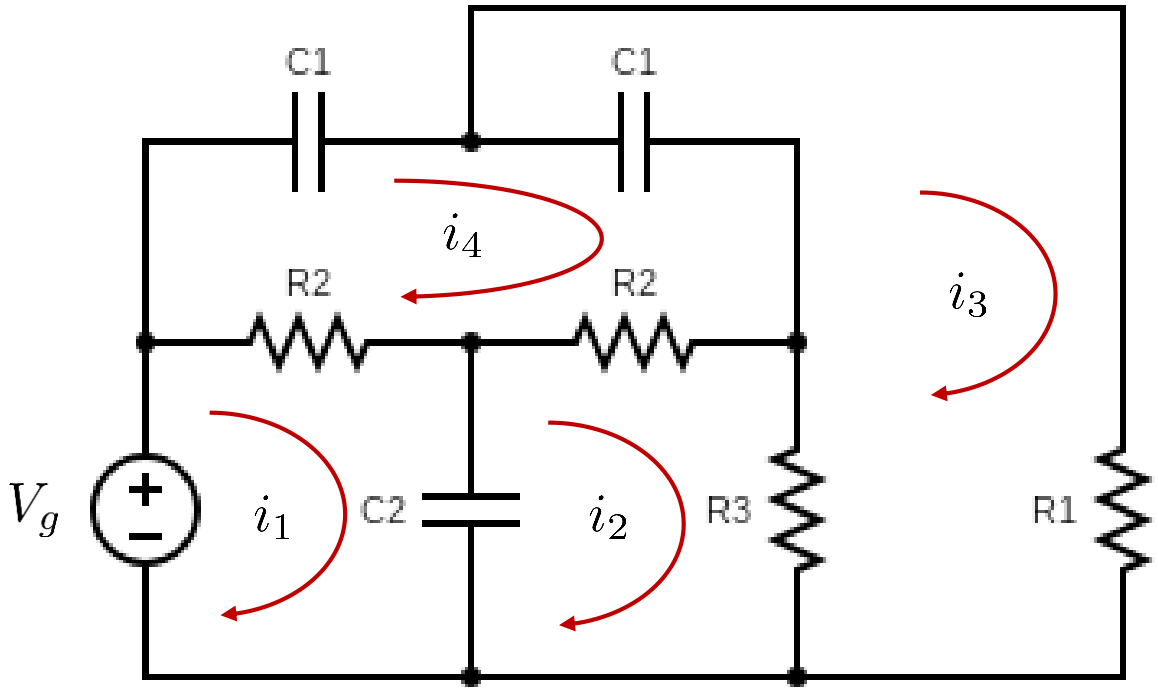
$$\frac{v_3 - v_2}{R_2} + \frac{v_3}{R_3} + C_1 \frac{d}{dt}(v_3 - v_4) = 0$$

$$\frac{v_4}{R_1} + C_1 \frac{d}{dt}(v_4 - v_3) + C_1 \frac{d}{dt}(v_4 - v_1) = 0$$



Loop Analysis

Reinforcement Example:



Loop 1: $i_1 R_2 + \frac{1}{C_2}\int (i_1 - i_2)dt - v_1 = 0$

Loop 2: $i_2 R_2 + \frac{1}{C_2}\int (i_2 - i_1)dt + (i_2 - i_3)R_3 = 0$

Loop 3: $\frac{1}{C_1}\int (i_3 - i_4)dt + i_3 R_1 + (i_3 - i_2)R_3 = 0$

Loop 4: $\frac{1}{C_1}\int i_4 dt + \frac{1}{C_1}\int (i_4 - i_3)dt + (i_4 - i_2)R_2 + (i_4 - i_1)R_2 = 0$

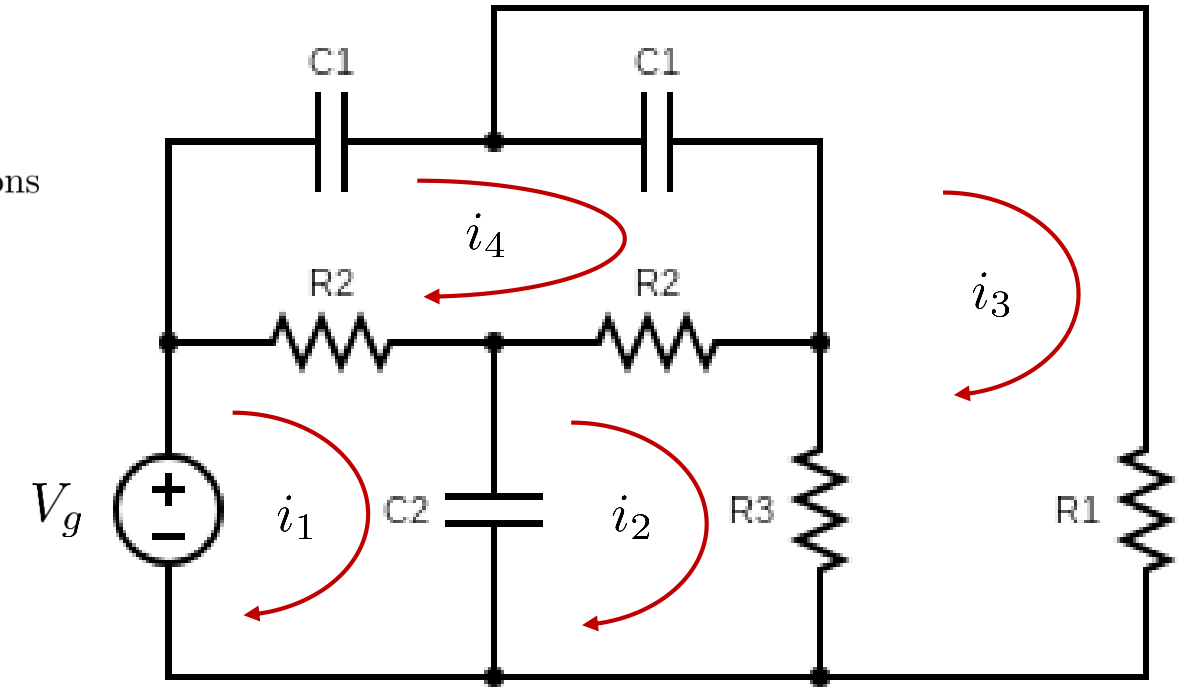
Loop Analysis - Matrix Form

Example:

By rearranging the terms in the loop equations, we can write the equations in the matrix form

$$\mathbf{Ai} = \mathbf{v}$$

$$\mathbf{v} = \begin{bmatrix} V_g \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad \mathbf{i} = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix}$$



$$\mathbf{A} = \begin{bmatrix} R_2 + \frac{1}{C_2}\int(\cdot)dt & -\frac{1}{C_2}\int(\cdot)dt & 0 & -R_2 \\ -\frac{1}{C_2}\int(\cdot)dt & R_2 + R_3 + \frac{1}{C_2}\int(\cdot)dt & -R_3 & -R_2 \\ 0 & -R_3 & R_1 + R_3 + \frac{1}{C_1}\int(\cdot)dt & -\frac{1}{C_1}\int(\cdot)dt \\ -R_2 & -R_2 & -\frac{1}{C_1}\int(\cdot)dt & 2R_2 + \frac{2}{C_1}\int(\cdot)dt \end{bmatrix}$$

$a_{\ell,k}$ - entry of the matrix at ℓ-th row and k-th column

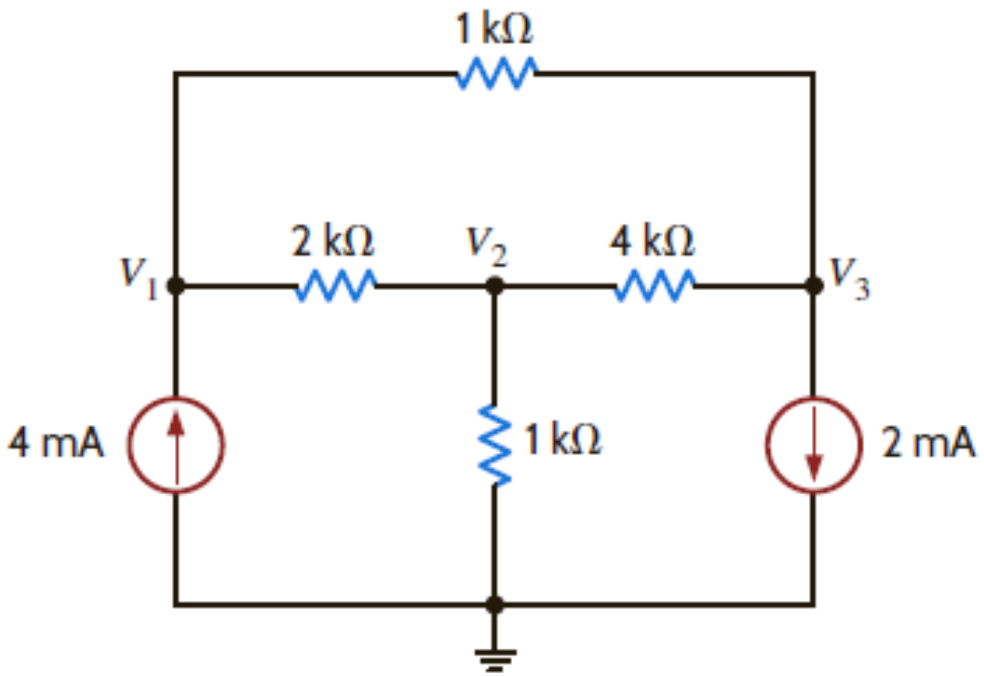
Interpretations: $a_{\ell,k}$ contains the terms for the elements shared between loop ℓ and loop k.

$\mathbf{A}$ is symmetric if there are no controlled sources in the circuit.

Nodal Analysis

Matrix Formulation Reinforcement - Example:

Determine V_1, V_2 and V_3.



$$\frac{v_1 - v_2}{2k} + \frac{v_1 - v_3}{1k} - 4m = 0$$

$$\frac{v_2 - v_1}{2k} + \frac{v_2 - v_3}{4k} + \frac{v_2}{1k} = 0$$

$$\frac{v_3 - v_1}{1k} + \frac{v_3 - v_2}{4k} + 2m = 0$$

By rearranging the terms in the nodal equations, we can write the equations in the matrix form

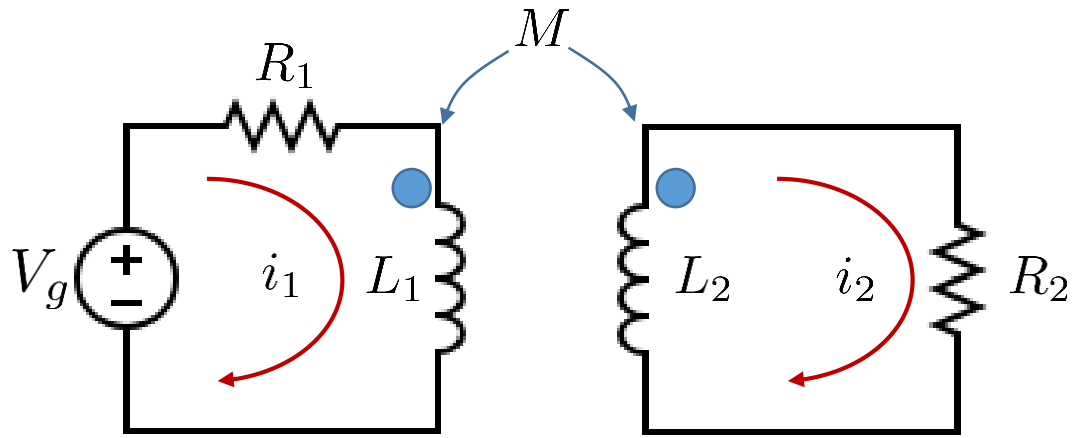
$$\mathbf{Bv} = \mathbf{i}$$

$$\mathbf{B} = \begin{bmatrix} \frac{1}{2} + 1 & -\frac{1}{2} & -1 \\ -\frac{1}{2} & \frac{1}{2} + \frac{1}{4} + 1 & \frac{1}{4} \\ -1 & -\frac{1}{4} & \frac{1}{4} + 1 \end{bmatrix} \quad \mathbf{v} = \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \quad \mathbf{i} = \begin{bmatrix} 4 \\ 0 \\ -2 \end{bmatrix}$$

Kirchhoff's Voltage Law for Coupled Inductors

Example: (Circuit with multiple parts)

This circuit has 2 parts.



Loop 1 Equation:

$$R_1 i_1 + L_1 \frac{di_1}{dt} - V_g - M \frac{di_2}{dt} = 0$$

This term is due to the coupling between the inductors.

Loop 2 Equation:

$$R_1 i_2 + L_2 \frac{di_2}{dt} - M \frac{di_1}{dt} = 0$$

Use dot convention to determine the direction of polarity of this induced voltage in L_1 due to the current in the second loop.

KCL, KVL – Number of Equations

Connection with graphical representation

We analyse the electric circuit by forming network equations governed by KCL and KVL.

We should learn to use these laws **intelligently** to formulate **minimum** number of **independent** equations describing the network **completely.**

KCL – Nodal Analysis
KVL – Loop Analysis

To determine the number of equations obtained by using KCL or KVL, we use the graphical representation of the circuit.

For a circuit with **n** nodes and **b** branches (or edges)
- KCL: number of equations = **n-1**
- KVL: number of equations = **b-(n-1)**

For a circuit with **p** parts
- KCL: number of equations = **n-1+(p-1)**
- KVL: number of equations = **b-(n-1)+(p-1)**

Recall **b-(n-1)** represents the number of chords to be removed from the graph of the circuit to obtain its tree.